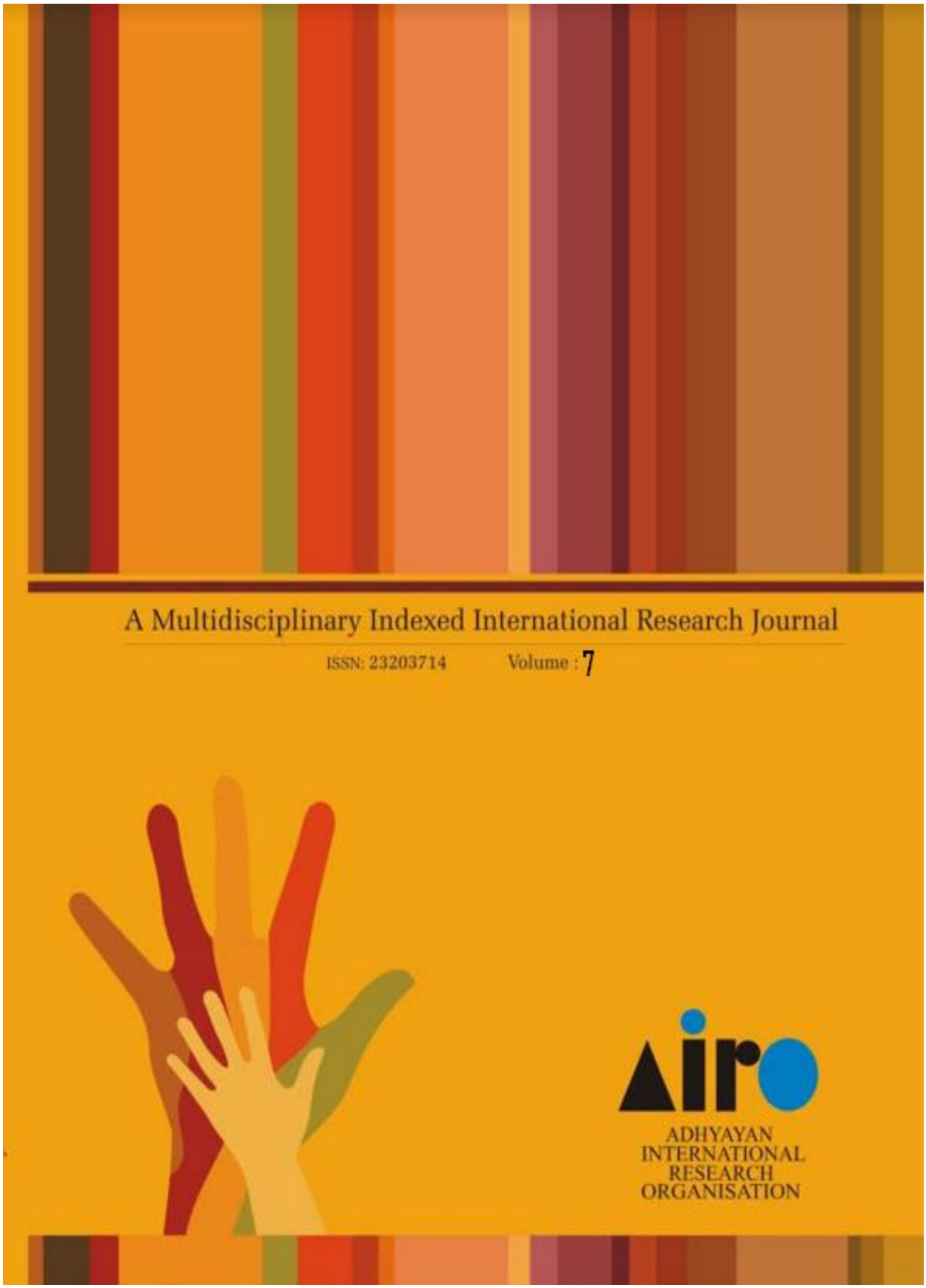
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STUDY ON DESIGN AND DEVELOPMENT OF LOW POWER BINARY AND HARDWARE EFFICIENT DECIMAL ADDERS

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ABSTRACT

This article presents a novel architecture for hardware efficient binary represented decimal addition. We extend the two operand ripple carry addition by one with the third input being constant. The addition technique is made fast by generating flag bits appropriate to the constant added. The third constant in case of our proposed design is 6 (0110) for converting the outputs exceeding 9 to Binary Coded Decimal (BCD) number. The proposed BCD adder has been designed using VHDL code and synthesized using Altera Quartus II. Experimental results show that the proposed design outperforms the previous researches in terms of power dissipation and area FPGA Implementation of Low Power Hardware Efficient Flagged Binary Coded Decimal Adder

INTRODUCTION

Adders are the key components of ALUs and MAC utilized as a part of picture and signal processing architectures as they lie in the critical path. Adder performance can be enhanced by decreasing the delay of carry propagation chain or basic adder cell. This can be tended to by either enhancing the structure of the 1-bit FA which is one of the basic cells in adders, for example, the carry select or carry skip, and in addition the building piece of the RCA, since a n bit RCA is formed by n 1-bit FAs, or by utilizing enhanced fast adder architectures, for example, Conditional Sum Adders (CSUAs) or CLAs

The adder proposed by Hassoune et al (2010) utilizes hybrid logic combining PT logic and BBL for sum and carry squares separately. The logic styles utilized as a part of this adder are less complex and their combination requires less transistors compared to CMOS FA and CPL FA (Hassoune et al 2010). However BBL-PT FA has high delay since the gate of the level restorer PMOS in sum piece is driven by supplement of yield, bringing about stride yield (Hassoune et al 2010). A Low Power Full Adder(LPFA) using ALDC is a hybrid FA, which combines pseudo NMOS for carry and PT logic for sum is proposed and discussed

DESIGN OF LOW POWER FULL ADDER USING ALDC (LPFA-ALDC)

In this segment another structure of hybrid FA is designed by consolidating Pseudo NMOS logic and PT logic. Additionally, another circuit for driving the level reestablishing weak PMOS transistor is designed and executed in the LPFA. An examination between proposed LPFA, LPFA - ALDC, and its counterparts viz., static CMOS FA, CPL FA, CMOS-BBL hybrid FA and BBL-PT FA are done utilizing TSPICE utilizing 180nm technology file

DESIGN OF HARDWARE EFFICIENT FLAGGED BINARY CODED DECIMAL ADDER

Decimal adder is the critical part of ALUs intended for business and commercial applications. They are the key components as they lie in the critical path of the preparing architecture and decide the overall execution of the system

Overview of BCD Addition

In electronic system, BCD is an encoding for decimal numbers in which every digit is represented by its own particular binary grouping. It enables simple transformation to digits and results in faster calculations. At the point when BCD numbers are included, each sum digit ought to be changed in accordance with skip the six unused codes. For example, the additions of two decimal digits in BCD, together with a conceivable carry from a past minimum significant pair of digits (expecting most extreme incentive for input digits) viz., 9 + 9 +1 would bring abo.The equal binary aggregate will be in the range 0 to 19 represented in binary as 0000 to 10011 and BCD as 0000 to 1 1001(the initial 1 being carry

and next four bits being BCD digit sum). For the binary sum equivalent to or under 1001 the relating BCD digit is the same. However when the binary sum surpasses 1001, the outcome is invalid BCD digit. The expansion of 6(0110)2 to the binary entirety converts it to the correct digit and furthermore delivers carry (Morris Mano 2001) Figure.1 demonstrates the block diagram of a 1 digit BCD adder (Morris Mano 2001) in light of the above methodology.

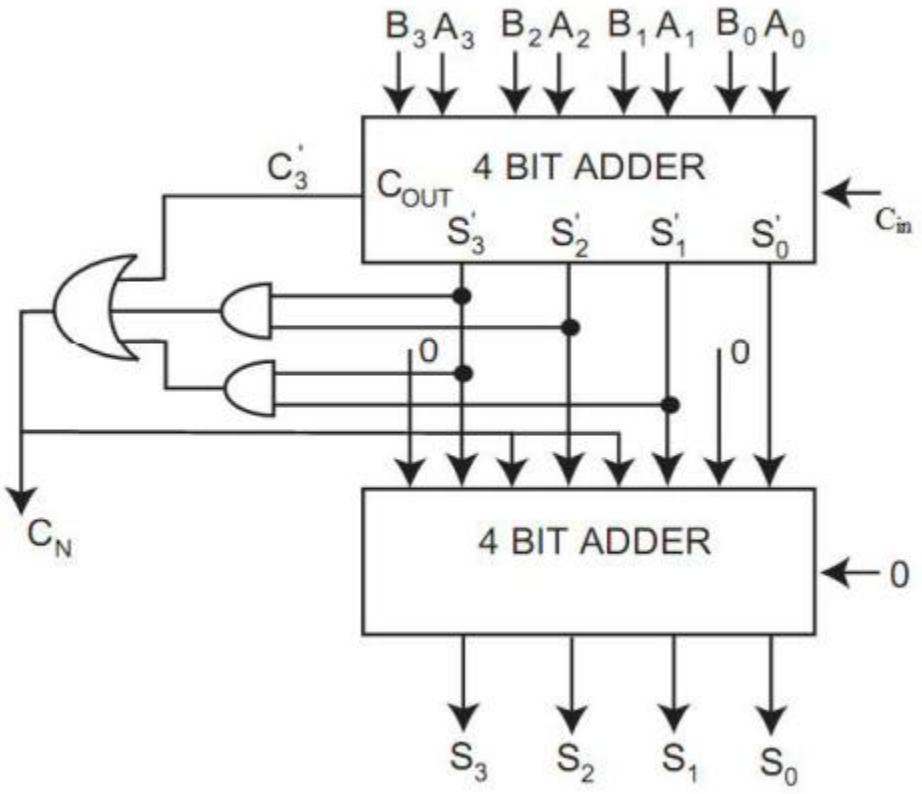

Figure.1 Block diagram of BCD adder

Proposed Flagged BCD Adder

The hardware efficient BCD adder utilizes flagged binary addition method proposed by

Dave et al (2010). The different blocks of the Flagged BCD adder are 4 bit RCA, Excess 9 indicator, flag bit calculation block, flag reversal block and four 2:1 multiplexers as appeared in Figure.2. The input bits A3A2A1A0 and B3B2B1B0 are fed to the principal arrange binary adder. The sum output S(S3'S2'S1'S0') and complete Co of this stage is encouraged to Excess 9 detector appeared in Figure 3 On the off chance that the sum S(S3'S2'S1'S0') is not exactly or equivalent to 9 the Cout of Excess 9 finder will be zero and the sum S(S3'S2'S1'S0') will be gone out through the multiplexer.

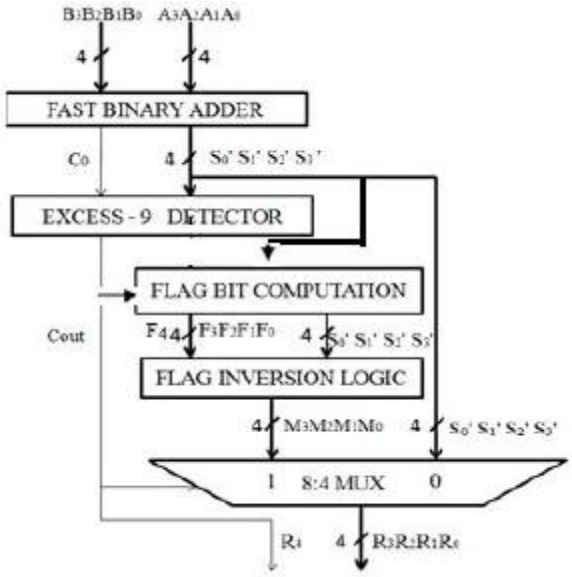

Figure 2 Block diagram of flagged BCD adder

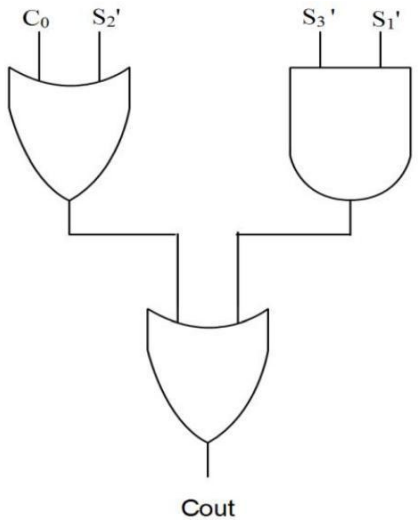

Figure 3. Schematic of Excess-9 detector

If the sum $S(S_3'S_2'S_1'S_0')$ exceeds 9, the C_{out} of Excess 9 detector will be 1 and the sum bits will be passed through the flag bit computation block shown in Figure.4 to generate intermediate carry bits $d_{4,}d_{3,}d_2$ and d_1 shown in Equation (3.7) to Equation(3.10)

$$d_1=0 \quad (3.7)$$

$$d_2= S_1' \quad (3.8)$$

$$d_3=d_2 + S_2' \quad (3.9)$$

$$d_4=d_3\& S_3' \quad (3.10)$$

The intermediate carry bits $d_{4,}d_{3,}d_2$ and d_1 are then used by the flag bit computation block to generate flag bits F_0, F_1,F_2,F_3 and F_4 shown in Equation (3.11) to Equation (3.15).

$$F_0 =0 \quad (3.11)$$

$$F_1= 1 \quad (3.12)$$

$$F_2=\text{not}(d_2) \quad (3.13)$$

$$F_3=d_3 \quad (3.14)$$

$$F_4=d_4 \quad (3.15)$$

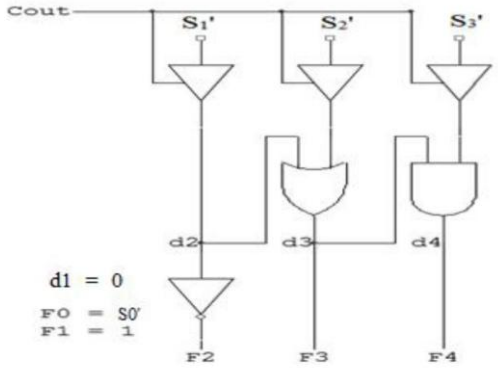

Figure 4. Schematic of carry and flag bit computation block

The flag bits F0,F1,F2,F3 and F4 and sum S(S3'S2'S1'S0') are gone through flag reversal logic appeared in Figure.5 to create the BCD output M3M2M1M0 for S(Co S3'S2'S1'S0')which surpasses 9. The M3M2M1M0 of the flagged reversal block is the other inputto the multiplexer which is passed out for Cout is 1

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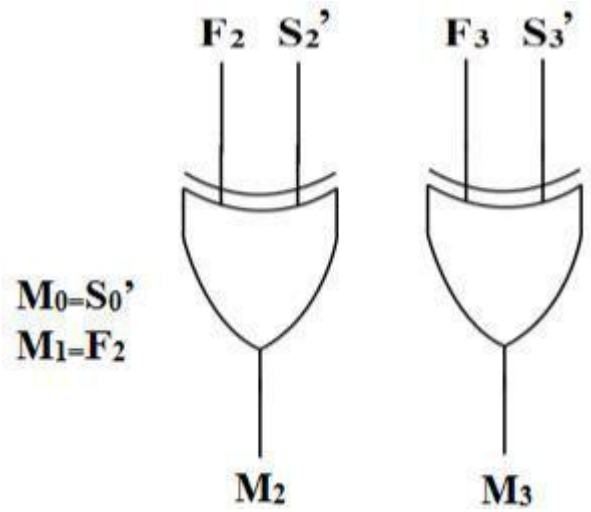

Figure.5 Schematic of flag inversion logic

Performance Analysis

The Flagged BCD adder is depicted utilizing structural VHDL to deliver gate level net list and synthesized utilizing Altera Quartus II. The proposed BCD adder is assessed utilizing Carry Skip (CSK) adder (Cha and Swartzlander 2000) and CSLA (Ramkumar and Kittur 2012) for the primary stage addition. Regular BCD adder (Morris Mano 2001), Correction free BCD adder (AlKhaleel et al 2011), Carry skip BCD adder (Thapliyal et al 2006) are utilized for comparison. The zone, delay and total power dissipation comes about for 1 digit adder plans are appeared in Table 1. A plot of area of these adders is appeared in Figure 6.

Table 1Comparison of area, delay and power dissipation of flagged BCD adder and state-of-the art designs for 1 digit

Parameters / BCD Adders	Area (Number of Logic Elements)	Delay (ns)	Total power dissipation (mW)	Static power dissipation (mW)
Conventional (Morris Mano 2001)	11	15.230	144.06	80.04
Correction free (AlKhaleel et al 2011)	29	13.326	147.02	80.05
CSK(Thapliyal et al 2006)	15	11.500	138.36	80.02
Proposed-Using CSLA	13	12.303	146.43	80.04
Proposed-Using CSK	9	12.984	146.31	80.04

This is because of the long carry generation(Cout) way which is 1 OR abundance of 4 XOR delays in Conventional BCD adder (Morris Mano 2001) and more number of stages utilized as a part of Correction free BCD adder (AlKhaleel et al 2011). What's more the proposed BCD adders show better power dissipation performance contrasted with redress free BCD adder design.

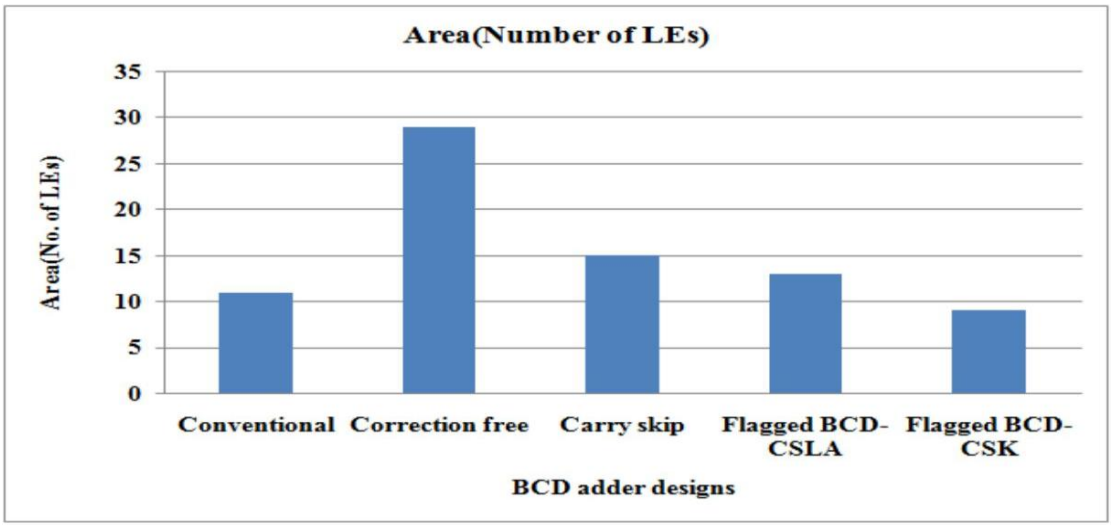

Figure 6. Area of 1 digit decimal adders

Implementation of the Flagged BCD Adder for 2 Digit Addition

To determine the functionality of the proposed BCD adder an implementation in 2 digit addition is done and is shown in Figure 7.

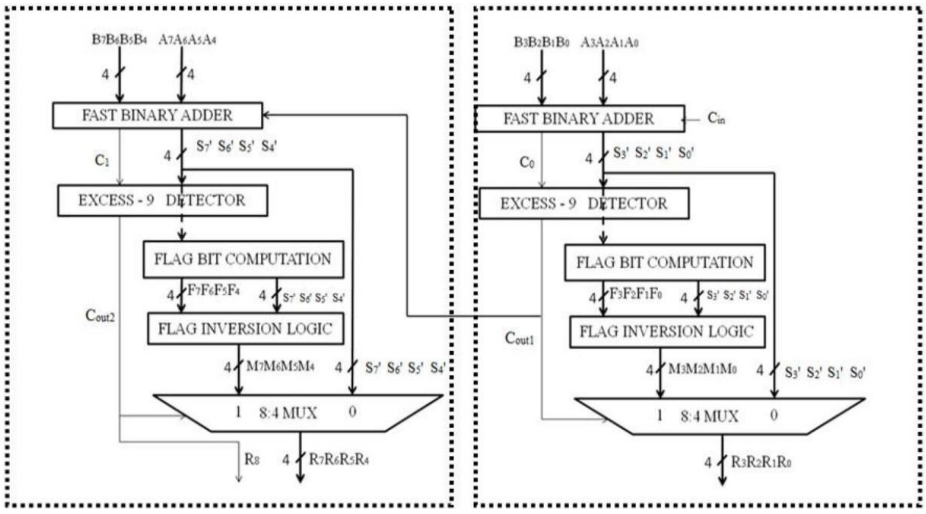

Fig.7 Flagged BCD Adder for 2 Digit Addition

The carry out of the principal digit adder (Cout) is utilized as the carry input of starting stage adder of second digit adder. The carry spread time for a two digit execution is 7 AND + 14 OR gate delays

Be that as it may, LPFA and LPFA-ALDC indicate poor static power dissipation compared with the state-of the art designs which should be concentrated for advance improvement.

CONCLUSION

In this chapter efficient design of a LPFA and a BCD adder are done. The design of LPFA is finished utilizing Pseudo NMOS logic for carry and PT logic for aggregate. An enhancement of the LPFA has been done by executing an ALDC for driving draw up PMOS transistor to lessen the static and total power dissipation. Recreations utilizing TSPICE in 180 nm technology have demonstrated that LPFA-ALDC and its essential version- LPFA exhibits critical diminishment in total power dissipation when contrasted with past approaches specified in literature. Also, the ALDC actualized adder design performs better regarding static and total power dissipation contrasted with the fundamental form. A usage of the LPFA, LPFA-ALDC designs in 4-bit CSLA circuit demonstrated better total power decreases contrasted with 4-bit CSLAs executed with adders utilized for comparison. A usage in complex designs, for example, ALUs and MAC, could completely understand the advantages of proposed Pseudo NMOS-PT adder ALDC.

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